

BACKGROUND OF THE INVENTION

This invention relates generally to portable data collection and processing terminals for use in a Radio Frequency (RF) communication network, and, more specifically to portable terminals supporting a variety of RF transceivers and associated antenna systems. Additionally, this invention relates to methods in which a portable terminal gains access to the RF communication network.

In particular, portable data processing terminals have taken an increasingly significant role in business environments. For example, battery powered, hand-held data collection terminals are used extensively for inventory control in warehousing and merchandising operations. Other uses of such terminals include invoicing, delivery route management, order taking and return control operations -- as might be found in automobile rental operations.

In many business environments, portable data processing terminals often need to communicate in real-time with other portable terminals, peripheral devices, work stations, and host computers. To meet such communication needs, a variety of mixed hard-wired and wireless communication networks with associated communication protocols have been developed, each addressing the specific requirements of a given business environment. In the process of such development, portable terminals have undergone tailoring of both hardware and software to fully support a specific communication network and associated protocol.

As a result of such tailoring, each type of portable data

collection terminal is generally only capable of operating in a single type of business environment. Tailoring also results in unreasonable additional costs associated with developing, manufacturing, documenting, etc., each variety of portable data collection terminals.

More specifically, each portable data collection terminal includes a built-in radio transceiver. The built-in transceiver operates pursuant to only one of a variety of types of RF (Radio Frequency) communication characteristics, characteristics that are dictated per FCC (Federal Communication Commission) specification.

The choice of the type of radio transceiver, i.e., the type of RF communication characteristics, to build-in is based on the nature of the business environment. For example, a digital cellular radio might be chosen in a environment having great distances between the radio and the destination transceiver. Similarly, data might be exchanged using a single channel UHF (Ultra-High Frequency), direct-sequence spread-spectrum, or frequency-hopping spread-spectrum band. Each of these bands have particular characteristics which make them attractive for a given business environment, and each generally requiring a different transceiver.

After choosing the appropriate radio transceiver, an appropriate antenna must also be selected. Each type of transceiver often requires a different type of antenna based on the corresponding RF communication characteristics, the shape of the portable terminal, and the business environment at issue.

Thus, there is need to provide a portable data collection terminal capable of easily supporting any of the plurality of types of radio transceivers and associated antennas, minimizing needed modifications to the terminal's hardware and software design.

In addition, to support real-time access to a communication network, each portable data collection terminal needs to establish and maintain radio connectivity to the network. However, portable terminals must also address conflicting concerns of battery power conservation, i.e., maintaining connectivity places a substantial load on battery power. Moreover, the mobile nature of portable terminals also presents difficulties in maintaining connectivity. It would therefore be desirable to implement communication protocol techniques which address power saving and mobility concerns while providing virtually real-time access to the communication link.

Thus, an object of the present invention is to provide a modular hardware and software radio design for a portable data collection terminal which supports multiple types of radio transceivers and associated antennas.

It is also an object of the present invention to provide for the selection of ones of a plurality modular radio transceivers for use by a portable data terminal, the selection of which addresses the specific concerns of a given business environment.

Another object of the present invention is to provide for the selection of ones of a plurality of modular radio transceivers for use by a portable data terminal, wherein each modular transceiver selected isolates the data collection terminal from transceiver

specific operations by providing hardware and software control over such functions.

A further object of the present invention is to provide a communication protocol which address power saving and mobility concerns while providing virtually real-time access to the communication link.

Another object of the present invention is to provide a communication protocol for use by a portable data collection terminal which minimizes transmission collisions while providing for virtually real-time access to the communication network.

Another object of the present invention is to provide a communication protocol for use by a portable data collection terminal which eliminates the need for random number generation and random back-off techniques.

A further object of the present invention is to provide an improved computer device apparatus for connecting a removable card type radio to a protected, interchangeable, environmentally sealed antenna which uses contacts located on the housing of the radio card.

An object of the present invention is to provide an improved antenna connector for use with radio cards which can be inserted into various computer devices.

An object of the present invention is to provide an antenna cap, for use with computer devices utilizing radio cards, which is reliable, economical and easy to use.

A further object of the present invention is to provide an

antenna cap whereby an appropriate antenna will be connected to a radio card by selectively positioning the antenna contacts on the radio card.

Another object of the present invention is to provide an antenna cap whereby a radio card may simultaneously connect to and utilize more than one radio antenna, and where the radio card may contain more than one type of radio transceiver.

A further object of the present invention is to provide an improved antenna connector whereby an appropriate antenna(s) will be connected to a radio card by selectively positioning the antenna contacts on the radio card.

A further object of the present invention is to provide an improved apparatus which utilizes only one set of contacts on a radio card or modem card and uses a switching matrix to connect the radio card or modem card to the appropriate antenna or telephone line.

Other objects, advantages, and novel features of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

SUMMARY OF THE INVENTION

These and other objects of the invention are achieved in a portable data collection terminal comprising a first and second data processing unit as well as a radio transceiver selected from a plurality of transceivers. The first processing unit is capable of operating at its own set of communication software routines. Further, each of the plurality of radio transceivers has different operating characteristics. The second processing unit is capable of isolating the first processing unit from the differences in the operating characteristics of the plurality of radio transceivers.

In one embodiment of the portable data collection terminal, the first processing unit is contained in a base module while the second processing unit and the selected radio transceiver are located in a communication module. In another embodiment, antennas are connected to the base module, and the portable data collection terminal unit includes a means for selectively interconnecting one of the antennas to the communication module. In a further embodiment, a preinstalled antenna is connected to the base module. The portable data collection terminal includes an antenna connector capable of connecting a variety of external antennas as well as a means for selectively interconnecting the preinstalled antenna or the antenna connector to the selected radio transceiver.

The objects of the invention are also achieved in a portable data collection terminal that operates in a communication network having a first and second subnetwork. The portable data collection terminal comprises a base processing unit and a communication

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processor, as well as a first and second radio transceiver selected from a plurality of radio transceivers. The base processing unit is capable of operating at its own set of communication software routines. Further, each of the plurality of radio transceivers has different operating characteristics. The communication processor is capable of isolating the base processing unit from the differences in the operating characteristics of the first and second radio transceivers.

In one embodiment, the base processing unit is contained in a base module of the portable data collection terminal. The data collection terminal also has a communication module that contains the communication processor and the first and second radio transceivers.

The objects of the invention are also achieved in a method used by a second device for beginning a data exchange over an RF communication link with a polling device. (The polling device having an interpoll gap time.) The method comprises identifying that an RF communication link is clear throughout a period which is at least as long as the interpoll gap time and transmitting a request for poll frame. In one embodiment, the method also includes generating a first pseudo-random time which is also at least as long as the interpoll tap time. The channel is then sensed for a time substantially shorter than the first pseudo-random time. Such sensing is repeated until the channel is detected as being busy, or until the channel is detected as being clear at every sense until the first pseudo-random time is reached.

If the channel is busy, a second pseudo-random time delay backs-off is executed and the process beginning at the generation of the first pseudo-random time is repeated. If the channel is clear for the entire first pseudo-random time, a request for poll is transmitted.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic pictorial representation of a modular data collection terminal unit to which the present invention applies and showing schematically physical representation of modules of the data collection terminal;

FIG. 1A is a schematic diagram of functional blocks for illustrating major functional elements of a base module and a respective data and communications module of a data terminal in accordance with the present invention;

FIGS. 1B and 1C are diagrams illustrating the modularity of the software protocol stack used by the data terminal in accordance with the present invention;

FIG. 2 is a schematic diagram of functional interfaces among various modules of the data collection terminal shown in FIG. 1.

FIG. 3 is a schematic diagram of a control microprocessor, illustrating data bus terminals for synchronous communications.

FIG. 4 is a sequencing diagram showing schematically occurrences of a module-initiated communication sequence in accordance with features of the invention;

FIG. 5 is a further sequencing diagram illustrating schematically occurrences of a controller-initiated communication in accordance with features of the invention;

FIG. 6 is a schematic diagram of an alternate embodiment of the invention showing major functional elements and their interaction with a power saving microprocessor control circuit in accordance with the invention;

FIG. 7 is a schematic diagram showing typical, frequency related current characteristics of a control microprocessor device of the circuit shown in FIG. 5;

FIG. 8 is a schematic diagram showing frequency related current characteristics of an application microprocessor device of the circuit shown in FIG. 5;

FIG. 9 is a flow diagram showing a desired interaction of the two microprocessor devices in FIG. 5 in accordance with the invention;

FIG. 10 is a diagram illustrating a protocol stack used in the data processing terminal of the present invention;

FIG. 11 is a diagram illustrating a local area communications network of the present invention;

FIG. 12 is a flow diagram illustrating another protocol embodiment used by the data processing terminal of the present invention for gaining access to the channel;

FIG. 13 is a flow diagram illustrating an alternate protocol embodiment used by the data processing terminal of the present invention for channel access which includes a retry counter;

FIG. 14 is a flow diagram illustrating an alternate protocol embodiment used by the data processing terminal of the present invention for channel access which uses periodic SYNC messages in roaming implementations;

FIG. 15 is a flow diagram illustrating another protocol embodiment used by the data processing terminal of the present invention for channel access which includes both periodic SYNC

messages and a retry counter;

FIG. 16 is a flow diagram illustrating a channel access protocol using a pseudo-random number generator according to another embodiment of the present invention;

FIG. 17 is a diagram of the basic communication structure used in the channel access protocol of the present invention;

FIG. 18 is a diagram illustrating an exemplary communication sequence according to the channel access protocol of the present invention;

FIG. 19 is a diagram showing an exemplary communication exchange and illustrating channel access using channel reservation scheme;

FIG. 20 is a flow diagram illustrating channel access using the channel reservation scheme of FIG. 19;

FIG. 21 is a perspective view of a radio card and a corresponding port for receiving the radio card built in accordance with the present invention;

FIG. 22 is a partial top plan view of a radio card and port for receiving the radio card with the radio card completely inserted in the port;

FIG. 23 is a partial side elevational view taken along line 3-3 showing the male/female pin connection of the radio card and the port of FIG. 22;

FIG. 24 is a front view taken along line 4-4 showing the female pin connections of the radio card of FIG. 21;

FIG. 25 is a perspective view of computer terminal showing the

slot for receiving the radio card;

FIG. 26 is front view taken along line 6-6 showing how a radio card to be inserted into the slot of the computer terminal of FIG. 25;

FIG. 27 is a perspective view of another radio card and a corresponding port for receiving the radio card built in accordance with the present invention;

FIG. 28 is a front view of another computer terminal and end cap capable of receiving a radio card;

FIG. 29 is a top view taken along line 9-9 of the computer terminal of FIG. 28;

FIG. 30 is a bottom view taken along line 10-10 of the computer terminal of FIG. 28 with the end cap removed;

FIG. 31 is a side elevation view taken along line 11-11 of the computer terminal of FIG. 28 with the slot for the radio card shown in dashed lines;

FIG. 32 is a partial top view taken along line 12-12 of the computer terminal of FIG. 31 showing the slot for receiving the radio card and the antennas;

FIG. 33 is a partial top view of yet another embodiment of a computer terminal built in accordance with the present invention showing the use of a switching matrix;

FIG. 34 is a back view of a computer device and radio card built in accordance with the present invention;

FIG. 35 is a side elevational view taken along line 2-2 of FIG. 34 of the computer device and radio card;

FIG. 36 is a partial top view taken along line 3-3 of FIG. 34 of the computer device;

FIG. 37 is a partial side elevational view of another computer device built in accordance with the present invention;

FIG. 38 is a top view taken along line 5-5 of FIG. 37 of the computer device showing the rubber cap inserted therein;

FIG. 39 is a partial vertical sectional view taken along line 6-6 of FIG. 38 showing a radio antenna embedded within the rubber cap;

FIG. 40 is a partial vertical section view taken along line 7-7 of FIG. 39 of the rubber cap;

FIG. 41 is a partial vertical sectional view of another embodiment of the present invention;

FIG. 42 is a partial vertical sectional view of still another embodiment of the present invention;

FIG. 43 is a partial back view taken along line 10-10 of FIG. 35 of the computer device;

FIG. 44 is a partial back view of still another embodiment built in accordance with the present invention;

FIG. 45 is a partial horizontal sectional view taken along line 12-12 of FIG. 44 of the band showing the shielded ribbon used to carry the antenna signals;

FIG. 46 is partial back view of a computer device of yet another embodiment of the present invention;

FIG. 47 is a diagram which illustrates the use of the portable data terminal according to the present invention which utilizes a

plurality of radios to access different subnetworks of an overall communication network.

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DETAILED DESCRIPTION OF THE INVENTION

Functional interconnections and power saving features of the present invention may be better understood from knowing how various building blocks or modules of a portable data collection terminal unit relate to each other. FIG. 1 shows a schematic arrangement of various physical modules or components that become integrated into the portable data terminal unit which is designated generally by the numeral 10. Hand-held terminals are of generally rectangular, elongate shape for accepted practical user friendliness. Thus the modular terminal unit 10 desirably has an elongate, rectangular shape. An upper module 12 provides a sensory or physical interface to an operator of the terminal unit 10. The module 12 is referred to as a keyboard and display module 12 and features a keyboard 14 which may be a typical alphanumeric keyboard, including also function keys and cursor manipulation keys as part of an integrated keyboard arrangement. The keyboard 14 may be, and desirably is, a submodule in itself, inserted and mounted into a mounting frame 15 of the keyboard and display module 12. In a typical manner, the depression of molded keytops 16 generally closes electrical contacts in a lower contact plane (not visible) of the keyboard 14. The type of keyboard 14 is, however, not critical and not considered limiting to the invention. The keyboard 14 being a selected one of a number of available keyboards is, however pertinent to the invention. For example, in one application the keyboard 14 may be preferred to be a twenty or a twenty-four key keyboard. Such a keyboard 14 comprises comparatively few keytops

16, the locations and functions of which are more readily learned and accepted by an operator. Such keyboards typically do not have alphabetical key functions. Thus for many record keeping and merchandising operations, the keyboard 14 having an array of twenty or twenty-four keytops 16 may be most desirable. In another operation, a greater number of keytops 16 may be required to display the letters of the alphabet, numbers, and to provide for the execution of various functions. Thus, a keyboard 14 having an array of fifty-six keytops 16 may be preferred. Numerous variations in the arrangement of the keytops 16 within the array of the keyboard 14 are additionally possible. Mechanical or touch sensitive keytops 16 may be employed. In fact, touch sensitive keyboards which are known in the art, and typically involve programming and bi-directional feedback, may be improved by interconnection features of the present invention which will become apparent from the detailed description as a whole.

The keyboard and display module 12 further includes an upper cavity 17 wherein a display screen 18 is disposed. The display screen 18 is preferably a state-of-the-art liquid crystal display, the liquid crystal display ("LCD") technology being well established in the art. A dot-addressable liquid crystal array screen 18 is ideal for "User friendliness" and versatility and permits the display of various alphanumeric characters and graphic symbols, as well as Chinese or Japanese character symbols. Of course, dot-addressable graphic representations are known to require a substantial level of data processing and memory storage

to permit the symbols to be displayed or moved about on the display screen 18 with reasonable speed. Long delays between the time that an operator pushes a keytop 16 to obtain data and the time that the requested data are displayed is considered "user unfriendly" and is commercially undesirable. A display technology which has become a standard is referred to as VGA technology. VGA screens are capable of fine gray scale or color resolutions. The display screen 18 would be part of a selected display screen module 19 of a number of available display screen modules.

FIG. 1A illustrates one embodiment of the data processing terminal of the present invention illustrating advantages in the modular design approach. The terminal utilizes a microprocessor controlled data transfer between the base module 201 and any of a number of data and communication modules which may include various radio transceivers such as frequency-hopping or direct-sequence spread spectrum radios, UHF (Ultra-High Frequency) radios, etc. The terminal 10 and all of its circuits, including those of attached modules, are powered by a power pack module 23 as described herein.

Specifically, FIG. 1A shows a block diagram of functions of the base module 201 and a typical data and communications module designated generally by the numeral 200. The base module 201 is operative in conjunction with a typical radio frequency transceiver provided by the data and communication module 200, for example. The base module 201 includes a typical keyboard module 202 interactively coupled to a microprocessor 204. A preferred

microprocessor is a 80C196KC device which is a 16-bit microcontroller 205 with on-chip masked ROM, RAM and built-in timers, ports, analog to digital converters and a serial interface 206. Thus, the microprocessor functions as a microcontroller and as an interface for communicating data and control signals to and from the base module 201. In addition to the on-chip memory capacity, an external ROM 207 and an external RAM 208 may be provided for additional data processing and communication capacity. Display controller and driver circuits 209 may be multi-chip circuits or may be integrated into a single device to drive the described LCD screen 210. A typical scanner interface 215 is coupled to a 9-pin connector 216, such as the referred to D-subminiature connector which may couple a laser scanner or CCD scanner to the base module 201 for data collection.

The data and communication module 200 is of particular interest in that an improved interfacing may be obtained by coupling communication between the data and communication module 200 and the base module 201 through a microprocessor 225, such as, for example an 80C51 microprocessor circuit. Typical on board ROM allows the microprocessor to be programmed to interact with a number of devices in accordance with the stored program. The microprocessor interacts with an interface circuit 226 which may be an analog or mixed analog and digital interface circuit. The program for interacting with the interface circuit 226 may also be stored within an on board ROM. The interface circuit 226 is coupled to a transceiver module 228. The microprocessor 225 may

also be coupled directly to a data collection interface 229 to receive data from a scanner for reading any number of different bar codes or for providing input data from other external sources. The operation of the microprocessor 225 for coupling data to the base module 201 allows various input patterns to be processed by any of specific operational protocols controlled by the microprocessor 225, such that the data input from the data collection circuit can be made the same from any of a number of devices. Also, with respect to the operation of the transceiver, the program for operating the microprocessor 225 may include particular address codes for data retrieval and data communication via the transceiver. The data sent via a data and control bus between the microprocessors 225 and 204 can emulate a uniform data transfer protocol to the base module 201. The addition of the microprocessor 225 in a data and communication module 200 thus increases the number of communications devices that may be represented by the data communication transceiver circuit or module.

The data and communication module 200 may be removed and replaced with a number of other modules. In those modules, the transceiver 228 may be, for example, any RF radio, such as a spread spectrum, UHF, or cellular transceiver. The commonality between all communication modules is the microprocessor 225 and the associated communication protocol back to the microprocessor 205 of the base module 201. In other words, the program function represented by the interface circuit 226 and interacting with the

microprocessor 225 permits the interactive control and data stream between the base module 201 and the data and communication module 200 to appear the same to the base module 201 no matter how the module 200 communicates.

The reference to the particular microprocessor circuits should not be considered limiting to the scope of the invention. The combination of two microprocessors interacting with each other, each controlling the environment of a respective one of two submodules such as the base module and the data and communication module permits an increased number of different components and functions to be used within the data system. The data collection terminal unit of the present invention is particularly designed for use in a mobile computer network. Such a network connects mobile interactive radio-equipped computers (such as the terminal unit 10) to an infrastructure of stationary computer devices.

Communication within the network is generally governed by software control through a grouping of software routines. Together, the software routines define an overall communication protocol for the network. The software groupings also define a stack of protocol layers; i.e., a protocol stack. The protocol stack divides the overall communication protocol into hierarchical layers of functionality.

FIG. 1B illustrates one embodiment of the software protocol stack used by the modular data collection terminal unit of the present invention. The protocol stack is split to illustrate that the functionality of the software is divided between the base

module 201 and the data and communication module 200. Specifically, the functionality of the upper layers of the protocol stack (i.e., sessions layer 251, transport layer 253, and network layer 255) is performed by the microprocessor 205 of the base module 201 while the functionality of the lower layers (i.e., data link layer 257 and physical layer 259) is performed by the microprocessor 225 of the data and communication module 200.

The sessions layer 251 performs general login functions, such as authentication of passwords, etc.

The transport layer 253 provides end-to-end connectivity within a mobile computer network. It recovers from lost data packets, discards duplicate data packets, and fragments and reassembles logical user messages. Essentially, the transport layer 253 provides a data pipeline between access points in terminal modes.

The network layer 255 provides end-to-end delivery of data packets within a mobile computer network. For example, if a spanning tree network offers the desired good network solution, the network layer 255 would (1) organize nodes in the network into a spanning tree; (2) route data packets along branches of the spanning tree; (3) provide a service for storing data packets for sleeping terminals (i.e. power management); (4) propagate lost terminal node information throughout the spanning tree; (5) maintain spanning tree links; (6) allocate and distribute network addresses; and (7) maintain and provide diagnostic network statistics.

The data link layer 257 controls access to the communication channel and is responsible for providing reliable transmission between any two devices in the network on both wired and radio links.

The physical layer 259 performs radio modem functions and is therefore very radio transceiver dependent.

As can be appreciated, the lower the level in the protocol stack, the more radio transceiver dependent the protocol becomes. Similarly, the lower the level, the more business environment specific the protocol becomes. Thus, a good dividing line for the protocol layers that exist in the communication module 200 is at the data link layer 257. This way, any communication module 200 supporting any type of radio transceiver can communicate with the common higher levels of protocol stack existing in the base module 201.

Alternatively, the dividing line might also be drawn at a higher level, for example, at the network layer 255, or at somewhere in between. For example, referring to FIG. 1C, a portion of the network layer which addresses the specific concerns of roaming portable terminals and power management might be migrated into the communication module 200. Such migration permits the communication module 200 protocol substack to be able to communicate with other higher level protocol stacks which do not directly support such network layer functionality.

Further detail regarding mobile computer networks and the above protocol is found in attached Appendix A, a Masters Thesis

entitled "Mobile Computer Network Architecture" authored by Robert C. Meier, a co-inventor herein.

FIG. 1C illustrates the compatibility of the lower layers of the protocol stack (i.e., that of the data and communication module 200 used by the data collection terminal unit of the present invention with a variety of standard protocol stacks. Particularly, the protocol of the data and communication module 200 is capable of interfacing with any personal computer (PC) based platforms that use a standard protocol stack. Such PC based platforms may include, for example, a Novell Ethernet Network or TCP/IP. The network layer protocol associated with the mobility of a terminal unit (i.e., specific spanning tree and power management functionality), data link layer, and the physical link layer is managed by the microprocessor 225 of the data and communication module 200. This protocol substack is stored in the interface circuit 226. Similarly, the substack containing the sessions layer transport layer and a majority of the network layer is stored in memory in the base module 201.

In an alternate embodiment, FIG. 2 illustrates a schematic diagram of functional interfaces among various modules of the data collection terminal unit of FIG. 1. As will become more apparent below, the embodiment in FIG. 2 expands on the concept explained in reference to FIG. 1A of splitting up the hardware functionality and software protocol layers of the terminal unit 10 to enable ease of radio transceiver substitution. FIG. 2 refers to a display screen module 20 which is similar in function to display screen module 19

discussed above, yet which may include selected differences to illustrate the advantages of the modular concept in combination with other features of the present invention. Display screens may vary in size or resolution or both, such that options among a number of display screen modules 19 may be made available to a potential user of the terminal unit 10. A display of an array of (128 by 240) pixels of, for example, (0.25 X 0.25) millimeter is an example of what is considered to be a desirable display screen resolution. Another screen array size may be (64 X 192) pixels, for example, of (0.35 X 0.50) millimeter per pixel.

The keyboard and display module 12 occupies most of the area of the terminal unit 10 which faces an operator when the terminal unit 10 is held and operationally used by the operator. Assembled to an underside 21 of the keyboard and display module 12 are preferably two major modules of the terminal unit 10. A first module is what is referred to as the terminal module 22. Whereas the keyboard and display module 12 is the major interface component between the operator and the terminal unit 10, the terminal module 22 is a major functional component of the terminal unit 10 itself, as will become apparent from the description herein. The terminal module 22 functionally controls the interaction of the various units or modules as described herein, and functionally is the control unit of the terminal unit 10. The terminal module 22 houses functional submodules and microprocessor circuits. A significant component is, of course, a power pack module 23. The power pack module may contain, for example, six AA type

rechargeable cells which may be arranged in a convenient flat arrangement and fitted into a battery end 24 of a housing 25 of the terminal module 22. The power pack module 23 supplies the power to various modules of the terminal unit 10, thus providing the capability for portable use of the terminal unit 10.

From the above description of potential choices of the type of display on the display screen 18, and further choices among keyboard arrangements of the keyboard 14, different requirements for electronic support circuits are indicated. One of the requirements to support the economical changing of functions is a means to provide a ready change in programmability of microprocessor circuits. Some module selections of the terminal unit 10 require less memory usage and different operational protocols than others. In accordance with a preferred embodiment, a memory module 27 may be selected as one of a number of differently programmed memory modules 27. However, in addition to being differently programmed, an alternate memory module 28 may include a different memory size (in cell numbers and in configuration). The terminal module 22 may further include an exchangeable memory card 30. The memory card 30 may be used to provide additional memory capacity as well as control programs for various desired functions of the various modules as described herein. The memory card 30 is schematically shown as being insertible laterally into a slot 32 of the housing 25 of the terminal module 22. However, the shown physical arrangement is but one of a number of equally desirable arrangements. An enclosed and

sealed arrangement for the memory card 30 is desirable to protect modules of the terminal unit 10 from the environment.

A peripheral I/O module 34 is shown at a lower or inner end 35 (see FIG. 1) of the terminal unit 10. The inner end 35 is typically pointed toward an operator of the terminal unit 10, as the unit is held in the operator's hand with the keyboard and display module 12 directed upward toward the operator. The I/O (Input-Output) module 34 may typically include externally of a housing 36 a standard RS-232 and RS-485 connector 37. FIG. 1 also depicts a round communication connector 38. The peripheral I/O module 34 provides an interface between the terminal unit 10 and such diverse peripheral devices as "docks". Docks may be batch transfer devices for transferring accumulated data, battery charging devices, or cables which may connect to a code scanner, for example. An RS-232 interface is typically connected to a printer, for example.

A serial I/O and scan connection module 41 may be attached at a longitudinally opposite outer end 40 (see FIG. 1) of the terminal unit 10. The scan connection module 41 is a high speed serial data communication module 41 which provides for serial data to be received in high volume from a scanner for example. Scanner data are typically received in a high density data string and require significant processing. As will become apparent below, a direct communication link to the data processing capability of the terminal unit 10 is provided through the scan connection module 41.

A further functional module is a communication module 44.

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Again in reference to FIG. 1, the communication module 44 may be disposed adjacent the terminal module 22 toward the outer end 40 of the terminal unit 10. The communication module 44 is selected from a group of available communication modules of distinct functions. The selection of one of the communication modules such as the communication module 44 in FIG. 1, may characterize or classify the operation of the terminal unit 10. For example, a communication module 44 may have been selected from a group of modules which include standard FM data radio transceiver modules, spread spectrum radio transceiver modules, modem communication modules, scanner device modules, or other data input devices. FIG. 2 shows a communication module 45 as an alternate to the physical representation of the communication module 44 shown in FIG. 1 to indicate a diversity of modules available for substitution. In further reference to FIG. 1, the communication module 44 is shown as having an antenna 46, indicating the selection being a transceiver unit for radio frequency real time communication with a data system. Such a data system typically includes a further transceiver station, not shown, with which the transceiver module 44 communicates. The operator of the terminal unit 10 also constitutes a second end of a communication link that is established by the operator's manipulation of the keyboard 14 and by the operator's visual perception and recognition of the data displayed on the display screen 18.

Referring now to FIG. 2, a functional schematic diagram of a combination of the physical modules discussed with respect to FIG.

1, or of alternate equivalents of the modules in FIG. 1, is shown. The modules with respect to which preferred physical positioning was discussed in reference to FIG. 1 are now shown functionally related in FIG. 2. It is to be noted that the schematic representation refers to functional or communication rather than electrical connections. The power pack 23 is typically coupled to power all electrically driven circuits of the terminal unit 10. The power pack 23 is functionally and physically coupled to the terminal module 22. While electrical power is distributed from the power pack 23 to all electrically powered or controlled modules of the terminal unit, the remaining power of the power pack is actually monitored by a function of the terminal module 22. The power pack 23 as the sole portable power source for the terminal unit 10 would, but for power saving provisions, experience a significant power drain during the operation of the terminal unit 10.

Power savings are implemented by selectively using circuit functions as they are needed. Accordingly, the terminal module includes preferably first and second microprocessors 48 and 49, respectively. The first microprocessor 48 is a data processing device and is also referred to herein as an application processor 48. The application processor may be any of a number of available microprocessors available. Desirably the application microprocessor 48 has the capability of processing data with greater word length or word width than the second processor 49. The term word width refers to the number of data bits that are

capable of simultaneously being processed, retrieved or stored. The application processor 48 is therefore one capable, for example, of processing a 16-bit or a 32-bit data word. The processing speed and clocking rate of the application processor 48 would desirably exceed that of the second microprocessor 49. At present, the more powerful microprocessors, such as the microprocessor 48, have higher power requirements than the second microprocessor 49. However, even with the higher power requirement during operation, power savings may be achieved by providing a rest state at which the microprocessor 48 is not clocked and thus deactivated.

The second microprocessor 49 is also referred to as a control processor 49. The second microprocessor controls the operation of the terminal module 22 and controls communication within the terminal module as well as among the various other modules of the terminal unit 10. The control processor 49 requires less power for operation than the application processor 48 for reasons that will become apparent. Control is an ongoing function. Because the operational speed of the control processor 49 is comparatively slower than that of the application processor 48, the operational power consumption of the control processor 49 is also lower than that of the application processor 48. The control processor 49 may be a Hitachi H8/330 type microprocessor device. The Hitachi H8/330 processor features on-board memory which is convenient for its intended operation as will be seen in reference to its operational modes as set forth herein. The H8 type processor is an 8-bit processor, capable of processing data in an 8-bit word length.

However, the control processor 49 need not be an 8-bit processor. In general, the word width processing capacity of the control processor 49 should be chosen to be relatively less than that of the application processor 48. The control processor 49 does not require the processing speed that is desirable for the application processor 48, and, processors with relatively low word width processing capacity (considering processors in general) require less processing power. It should be understood, however, that the specification of any particular device, such as the Hitachi H8-type microprocessor for the control processor 49, is for illustrative purposes only. The features and desired functions of the invention will be helpful to one skilled in the art to select any of a number of acceptable devices to function in the desired manner as described herein.

FIG. 3 shows a schematic block representative of signal terminals of the control microprocessor 49 which are pertinent to the preferred mode of implementing the present invention. In describing the significant signal and data terminals, a bar above a designation indicates that a low signal is active. Herein, the inverse or signal low active state is described with an "N" preceding the letter name at the respective signal term. To communicate among the various described modules, four signal leads of the control processor 49 define the leads of a communication bus 50 referred to herein as "MBUS". The MBUS 50 is a high speed synchronous serial data signal bus which may, and preferably does, operate at a signal rate of 500 kilo bits per second. The high

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speed data bus provides reliability advantages explained below. In a modular structure in which the modules are readily disconnected and reconnected to permit convenient changes during the manufacture of the final product, may reduce the reliability of the terminal unit 10. When reliability is decreased with each additionally coupled module, the advantages of modular structure are quickly dissipated. Compared to typical parallel data buses used to link components of electronic products or systems, the present system architecture of the modular terminal unit 10 requires significantly fewer contacts to interconnect the various modules. With fewer signal lines to manage, it becomes more feasible to protect each line from noise and interference effects by using well known shielding, impedance reduction and termination techniques thereby increasing the reliability of the terminal unit 10. As a result, the present invention is typically more reliable than modular systems with conventional parallel data transfer, due to the reduction in the interconnections among the various modules. FIG. 3 shows four signal terminals which constitute the MBUS concept. "MCLK" is the clocking signal which synchronizes the modular counterparts of the control processor 49. The clocking signal provides for a bit rate of 500 kilo bits per -second. The terminal labeled "MTXD" transfers data from the control processor onto the MBUS 50. The terminal labeled MRXD receives data from other modules over the MBUS 50. The low signal active "NMATT" is a control signal line which indicates that data will be communicated over the MBUS 50. These four lines effectively permit

the various modules to communicate among each other. A number of signal contention protocols are available to resolve potential collisions in data communication. It should be understood that any standard signal contention protocol may be modified if so desired to assign specific priorities for communication among the modules. For example, data received from a scanning operation may be accepted and processed on a priority basis. Keystroke inputs from the keyboard and display module 12 may be given priority over data flow from the communication module 45. Similarly, data messages received via radio transmission from an external master unit (not shown) may be given priority. Program altering instructions may be embedded within the message which affect future operations of the terminal unit 10.

Further with respect to FIG. 3, corresponding data lines interfacing with the application processor 48 are indicated as parallel signal lines DB0-7 and data lines A0-3. Data communication and control procedures between the control microprocessor 49 and the application processor 48 are further described with respect to alternate embodiments.

Referring again to FIG. 2, the application processor 48 is coupled to an asynchronous device or "UAR/T" function 51 with an output coupled to a serial port 52 of the serial I/O scan connection module 41. The serial I/O scan connection module 41 further includes a scan port 53 which links to the control processor 49 to communicate control signals, such as scan trigger signals, for example. The application processor 48 is further

coupled to a VGA adapter circuit or driver 54 for driving the display screen 20. The display screen function is processor intensive. Data processing operations are, therefore, managed directly through the application processor 48. The data processing operations performed by the application processor 48 are in most instances memory-usage intensive. Consequently, the application processor 48 is linked by a conventional data bus 55 directly to the memory module 28. The memory module 28 is shown as including representative data storage functions or circuits including a 16-bit word width system FLASH-programmable memory 56, a typical 16-bit word width random access memory 57 ("RAM"), and additional application FLASH-programmable memory 58, also preferably 16-bit word width. The 16-bit word width storage devices 56, 57 and 58 are preferred in conjunction with a 16-bit microprocessor device. Presently preferred 16-bit microprocessors are a Chips and Technologies F8680 device or an Advanced Micro Devices 386SXLV processor. The selection of other processors for the microprocessor 48 may require different types of memory devices or different word width or storage capacities than those described above.

The peripheral I/O module 34 may, as discussed with respect to FIG. 1, include standard connectors for coupling the module 34 to an external device. A particular device 59 may be a portable printer device, as shown in the function block 59 of FIG. 2, which may be mounted or coupled directly to the terminal unit 10. The peripheral I/O device, whether it is a printer or a reader or other

data input or output device, would functionally include a microprocessor 60. The microprocessor 60 is chosen to interact with the MBUS system. The microprocessor 60 is coupled in each described element to function as a terminal element, which is an interface communicatively coupling the respective logic circuits of the module to the MBUS. The microprocessor 60 receives control codes via the MBUS 50 and responds by activating or de-activating the power circuits of the respective module, or conditioning the module to receive or transmit data.

The communication module 45, which may be a modem or any of a number of available radio frequency transceiver modules, also includes a compatible microprocessor 60 which interfaces with a respective communication device 61 of the module 45. The communication device 61 may be a modem or transceiver device, for example. To be compatible with the MBUS data format of the other described modules. The keyboard and display module 12 also preferably includes its own interfacing microprocessor device 60. The keyboard and display microprocessor 60 is coupled to control various functions which are directly associated with the keyboard and display module 12. A particular function which may be conveniently controlled via the MBUS 50 and the respective control processors 49 and 60 is a backlight drive 62 for the display screen 20. Another function is a buzzer 63. The buzzer 63 may be activated to signal an incorrect key depression by an operator. The buzzer 63 may further be used to alert an operator when a charge and power control circuit 64 detects that the power pack 23

has become discharged and a backup battery 65 is being engaged, giving a user time to recharge or replace battery pack 23. The power control 64 may function to shut down the terminal unit 10 from further operation until the power pack has been recharged. In a preferred embodiment, power from the backup battery 65 would be maintained on the control processor to permit it to determine when power from the power pack 23 has been restored. The processor 60 of the keyboard and display module 12 may also control other input or output devices that may be coupled to the keyboard and display module 12. For example, a pen 66 may be coupled to the keyboard and display module 12 for use in connection with a pen stylus sensitive keyboard module 14 or in connection with a pen stylus sensitive display screen 20. In this latter instance, the display screen module 20 becomes an input device in addition to being an output device.

The application processor 48 and the control processor 49 are preferably controlled through a timing Application Specific Integrated Circuit 67 ("clock control ASIC"). The clock control circuit 67 may be driven from a single clock signal which is then divided to provide respectively different clocking rates to each of the processors 48 and 49. The implementation of the timing circuit 67 in a single circuit function is more efficient and provides synchronization among the components and modules. A second clock signal for implementing a real time clock may also be provided.

In addition to providing better reliability as discussed above, the MBUS 50 also provides more compact physical routing of

cables among the modules. Furthermore, control of the functions of the various described modules via the MBUS 50 provides power savings, as will be described more fully below in reference to FIGS. 4 and 5. To conserve power and prolong the operational time of the terminal unit 10 between changes or recharges of the power pack 23, the control processor 49 and the related MBUS module processors 60 place any module which is not in active use into dormant state.

The MBUS 50 communicatively interconnects the modules of the terminal unit 10, such as the peripheral I/O module 34, the communication module 45, the keyboard and display module 12 and the terminal module 22. Other modules that may be included in the active communication network of the MBUS 50 may simply be added as described herein. For each module, one of the microprocessors 60, having the data terminals of the microprocessor 49 shown in FIG. 3, namely MCLK, MTXD, MRXD and NMATT are coupled to the respective lines of the MBUS 50 to become part of the internal communication network of the terminal unit 10. The microprocessors 49 and 60 constitute the terminal elements of the communication network represented by the MBUS 50. For each module, the respective microprocessor 60, though it may be physically identical to the control microprocessor 49, functions as a subservient processor to the control processor 49. The microprocessors 60 become a communication interface between the MBUS 50 and the functional circuits of the respective module, whether the module is the communication module 45, the keyboard and display module 12 or the

into a low signal state. The low state of the NMATT line activates all processors 60 to receive an inquiry or instructions. At T1 in FIG. 4 all modules have been placed into the active state. During the time interval T1 to T2 the control processor sends a query or polls the activated modules over the MTXD line which is reserved for transmissions originating from the terminal module 22, i.e., from the control processor 49. The query would typically contain at least one byte of data, the quantitative translation of the byte of data indicating to the processors 60 that it is a query in response to one of the module processors 60 having driven the NMATT line to a low state. The query shown at 70 signals the processor 60 to transmit its data message over the MRXD line of the MBUS 50. At the onset of the data transmission 72 from the respective communicating module processor 60, the NMATT line is restored to a high state, placing all other modules back into the dormant condition. As shown in FIG. 4, the data communication may proceed for a variable length of time past the time state T2 at which the NMATT line has returned to a high state. Upon termination of data communication from the respective module processor 60 to the control processor 49, the control processor 49 sends a message 73 confirming correct receipt of the data message (at T3). Again the confirming data message contains at least one byte of information, the decoding of which would either indicate an error code or signal the correct receipt of the data message. At that time (at T3), the communicating module processor 60 and the control processor 49 also assume the power saving dormant state.

FIG. 5 describes a very similar event in which the control processor 49 drives the NMATT line to a low state. Again, all processors 60 assume an active state and all processors 60 receive a communication 75 of typically at least one byte of information from the control processor 49 during the time interval between T1 and T2. The information 75 contains an address of the module to which a data message from the control processor 49 will be directed. The respective module processor acknowledges its understanding of the address by a responding message 76 which may be translated by the control processor 49. In response to the receipt of the message the control processor releases the NMATT line, which assumes its normal high state and places all non-affected module processors 60 again into a dormant state. The control processor 49 then transmits its data message as indicated at 77 to the respective, previously addressed module processor 60. At the conclusion of the communication 77 from the control processor 49, the respective module processor acknowledges receipt of the communication 77 by its response 78. Once it is interpreted from the response 78 that the communication 77 has been received correctly, both the control processor 49 and the respective module processor 60 assume their dormant states. It is to be noted that the respective data messages shown in FIGS. 4 and 5 indicate durations of data messages. It is to be understood that the high and low states of other than the NMATT line indicate a time interval during which a great number of high or low states in synchronous time slots are transmitted essentially at the bit rate

of 500 kilo bits per second. This bit rate may include start and stop intervals.

In the described communication events, power consumption by the terminal unit 10 is minimized by providing for a quasi dormant state for substantially all functions of the various modules, such that electrical power is used in pulses during the described query states and only in spurts by certain modules during real time performances. The power saving features in communication from and to the various modules is further present in implementing highly power intensive data processing operations in the terminal module 22.

Referring to FIG. 6, the schematic diagram illustrates an alternate embodiment of the present invention where major functional logic and communications elements are coupled to and interact with the application processor 48 and the control processor 49 in a power-conserving microprocessor circuit 80. The circuit 80 may control the operations of, or be functional in the operation of, the terminal unit 10. The terminal unit 10 may interact as described with one or more distinct functional modules including communication modules, such as a transceiver communication module ("RADIO") shown at 81. Because the terminal unit 10 being portable, the physical circuits of the functional units or modules shown in FIG. 6 would typically be powered by the power pack or battery 23 (shown schematically in FIG. 2), which is illustratively included in the power management function ("POWER CONTR") 64. The microprocessor operated control circuit 80

comprises a combination of the application microprocessor 48 and the control microprocessor 49. The circuit 80 can also be two circuit portions that include specifically two microprocessor type subcircuits 48 and 49. Each of these subcircuits 48 or 49 are separately functioning microprocessor blocks, modules or separate microprocessor devices. In the preferred embodiment as described herein the devices are respectively an application processor 48 ("MP1") and a control processor 49 ("MP2"). It is advantageous to perform data processing operations at a comparatively higher speed and with a more powerful processor than is be desirable for relatively less complex control functions.

The term "data processing operation" is used herein in the sense of manipulating a series of binary codes according to programmed instructions to arrive at a desired result. Because of the great number of discrete binary operations required to perform many of the most common data processing functions, higher processor speeds and more complex or powerful microprocessor circuits of those typically available are more desirable for data processing operations.

In the now described embodiment, the application processor or data processing device 48 may be an "Intel 80C188EB" device which is "16-Bit" microprocessor device, operated at a preferred speed of 9.2 megahertz (MHz). At such preferred clocking speed of 9.2 MHz, the power consumption or operating current consumed by the data processing microprocessor device 48 is approximately 55 milliamps ("mA"). The control processor 49 may be a "Hitachi H8/325" device

which is an "8-Bit" microprocessor, operated at a speed of one-half of the speed of the data processing microprocessor 48, that is, 4.6 MHz. Because of the smaller physical size of the control processor 49 and the slower, preferred clocking speed, the power consumption or current required by the control processor 49 in its operational mode is only about 9 mA, that is less than one-fifth of the power consumed by the processor 48. In general, the control microprocessor circuit or the control microprocessor 49 desirably operates at a slower and less power consuming speed than the application microprocessor circuit or the application microprocessor 48. A one-to-two speed ratio for driving the respective microprocessors 49 and 48 is preferably chosen because of the power savings that are realized with respect to the portable terminal unit 10. Respective clocking circuits 82 and 83 ("CLK 1 and CLK 2") are shown as providing respective timing signal ports coupled to the respective processors 48 and 49 to drive the processors at the desired speeds as described.

Also, a functional arrangement of the separate clocking circuits 82 and 83 preferably may be replaced by the clock control circuit 67, as shown in FIG. 2. The clock control circuit 67 may be expanded in its function to include an interface circuit function between the processors 48 and 49 which includes data transfer as well as clocking functions. The clock control circuit 67 would include in such coupling arrangement a typical divide-by-two timing circuit function. An original 9.2 MHz clocking signal port and a signal port with the divided by two signal, comparable to the

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timing signal ports 82 and 83, would be coupled to the respective timing signal input ports of the processors 48 and 49, respectively, to drive the processors 48 and 49 at their respective speeds of 9.2 and 4.6 MHz. As mentioned above, a second clock may be coupled to the clock control circuit 67 to provide a real time clock.

As will become apparent from the further description, it is within the scope of the invention to integrate the distinct functions and operational characteristics of the separately identified microprocessor devices 48 and 49 into a single integrated device. The resulting integrated device 80 desirably includes respective interface functions, as further described herein, to implement the power-saving characteristics realized by the control circuit 80. Within such integrated device 80, the function of the application processor 48 is then performed by a first microprocessor circuit block or circuit portion, and the function of the control processor 49 is performed by a second microprocessor circuit block or circuit portion. These circuit blocks, portions or modules interact essentially in the same manner within the circuit 80 as the currently used microprocessor devices 48 and 49.

The control processor 49 may include in its commercial implementation, in addition to typical microprocessor registers and an arithmetic logic unit, such functional circuit blocks as ROM, RAM and communications ports. These circuit blocks may also be included in any integrated device 80, or their functions may be

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supplied by peripheral devices. As shown in FIG. 6, additional external memory 84 ("MEM") may optionally be provided to supplement such on-board memory 85 ("OM"), though for typical operations as further described herein, the external memory device 84 is not required. According to one embodiment, data communication between the processors 48 and 49 occurs via an interface circuit that includes, for example, two 8-bit data registers or latches described in greater detail below in relation to FIG. 6. It should be understood, however, that the control processor 49 may have a direct bus interface to enable direct coupling of the control processor 49 to the application processor 48. The coupled processors 48 and 49 are capable of bidirectionally passing data and control signals without the described two 8-bit data registers or latches. Also, data latches are generally considered temporary data storage devices. Data from one device are latched into a respective data latch to be retrieved by a second device. Although not preferred, it is contemplated that dual port memory may be used as an alternative to the latches described below.

The clock control ASIC function 67 shown in FIG. 2 should be understood to not only include the clocking signal coupling circuits to drive the respective application processor 48 and the control processor 49, but to further include the data interface or bus to permit the desired bidirectional data and control code communication between the processors 48 and 49 as further described herein. In further reference to FIG. 2, an integration of the processor devices 48 and 49 into a single device desirably may

include the described function of the interface and clock control circuit 67.

Referring again to FIG. 6, a first latch 86 ("LATCH 1") of the two latches is coupled through an 8-line parallel bus 87 to the microprocessor 49, and through a similar bus 88 to the microprocessor 48. Respective write and read lines 89 and 90 ("WRL1 and RDL2") provide control or trigger signals for the processor 49 to write data into the first latch 86 and for the processor 48 to read data from the latch 86. A handshake or control signal line 91 ("CHAR AVAIL 1") toggles between a high or "logic 1" to indicate to the processor 48 that data have been read into the first latch 86 by the processor 49 and a "logic 0" to signal that the processor has read or taken the data from the first latch 86. A second latch 92 ("LATCH 2") similarly stores an 8-bit data element written into the second latch 92 by the processor 48 over a second 8-bit write bus 93. A second read bus 94 transfers the data element stored in the second latch 92 from the latch to the second processor 49. The control or trigger signals for writing into or reading from the second data latch 92 are provided over trigger lines 95 and 96 ("WRL2 and RDL2"), respectively. A second handshake or control signal line 97 ("CHAR AVAIL 2") coupled to the second latch 92 and to the processors 48 and 49 also toggles between high and low signal states to indicate in the high state the availability of data in the second latch 92 and in the low state the completion of a read operation of the most recent data element by the control processor 49.

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A control signal line 98 carries a control signal generated by the control processor 49 which controls the duty cycle of the application processor 48. In reference to FIGS. 7 and 8, the current usage of the control processor 49 ranges between a high of 9mA in a typical operating mode and a low of about 7 mA in a typical "idle mode" at the preferred frequency of 4.6 MHz, (See FIG. 7, graphs 100 and 101, respectively). It should be realized that even while "idle", the control processor maintains power to internal memory and performs typical periodic monitoring functions, such as, for example, sampling a keyboard circuit 102 ("KB") for a "Depressed Key" signal or routinely monitoring the power management function 64 for a "Low Battery" indication. However, even when in the typical operational mode as indicated on the current vs. frequency graph 100, the control processor uses only about one-sixth of the current used by the application processor 48 in its preferred operational mode. On the other hand, when the application processor 48 is placed into an idle state (i.e., when it is not driven by a clocking signal), the required maximum current rating is 0.1 mA, as shown by the high-low indicated values at the 9.2 MHz frequency mark at and below graph 103 in FIG. 8. Graph 103 indicates the typical operating current consumption of the application processor 48. It should be noted that the application processor 48 could be deactivated by a complete electrical shut down of the device. However, because of the low non-clocked power or current draw of the application processor 48, the application processor function is preferably deactivated by

eliminating its clocking signal but maintaining the application processor 48 under DC bias. Removing the clocking signal from the application processor function achieves a desired power-down idle state while permitting the device 48 to be reactivated immediately by an appropriate "wake up" control signal from the control microprocessor 49.

Typical data processing operations performed by the application processor 48 require approximately 10 milliseconds of time and not more than 20 milliseconds on the average of all operations which are typically performed by the application processor 48. A more user friendly and practical response time may be obtained from the terminal unit 10 (and less power is required) when the application processor 48 performs substantially all data processing operations is subsequently immediately deactivated than if a single alternative microprocessor circuit were used operating at a higher rate and including sufficient computing capacity to perform all required functions in an appropriately short time. The combination of the application processor 48 and the control processor 49 amounts, only to an approximate increase in current usage of typically about ten percent, and in the extreme of no more than 20 percent, over the normal operating current level of the control processor by itself. The power required by the application processor 48 as controlled by the control processor 49 is about one fifth that required by the control processor 49 itself when it is operated continuously. However, the display speed and data manipulation speed of the terminal unit 10 essentially is the same

as if the unit 10 were controlled by the more powerful application processor 48.

The operating current requirement for the application processor 48 is directly related to the number of actively switching elements in each computational operation. Though having an interrupt function, the referred to 80C188EB processor 48 does not include, in contrast to the control processor 49, any internal memory devices. FIG. 6 consequently shows a data bus 55 of the processor 48 coupled to external memory devices, such as the flash electrically erasable and programmable read-only memory 58 ("FLASH EPROM"), a read-only memory 104 ("ROM") and a typical random access memory 57 ("RAM"). The ROM 104 is also the functional equivalent to the system FLASH memory 56. The data bus 55 further couples the application processor directly to the display module 20 ("LCD DISPLAY") of the terminal unit 10. The display module 20 may be a dot addressable LCD graphic screen module, for example. A direct data transfer by the high speed application processor 48 to the LCD screen is preferred because of the substantial amounts of data handling or processing that is required in updating a particular screen. For example, even a small graphic screen display, such as a screen of 48X100 pixels, requires that each of the pixels be updated on a continuous basis. Typically control circuits, which are part of the data display function of the module 20 and are not separately shown, and which may be specific to a particular screen display, may routinely re-apply currently displayed information dots in a cyclic refresh operation to the already identified pixels

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of the screen. However, any screen update, such as a simple display line scrolling operation, requires that each pixel of the screen be updated. To perform such updating of information in a power efficient and prompt, user-friendly manner, a data processing operation and the high speed passing of the updated data between the RAM memory 57 and the data display 20 is accomplished during a short operational activation of the application processor 48. More data processing with respect to the data display screen 20 may be required for routine menu operations. Menu operations are particularly desirable for such portable terminal units 10, in that the typical user may not be well acquainted with computer terminals. Well defined menu operations with a number of available menu levels may therefore significantly increase the usefulness of a terminal unit. In addition to requiring the normal display screen update, menu operators also require data base searing and data retrieval. The above-described operations the described microprocessor circuit (i.e., with the selectively activated data processing device 48 and the relatively smaller and slower control processor 49) may be used to perform the menu operations.

Selective activation and deactivation of the microprocessor circuit portion implemented by the data processing device or application processor 48 also provides power savings when the operating speeds of the two processors 48 and 49 are the same. However, such power savings do not appear to be as great as those realized by the embodiment described above.

The application processor 48 may also communicate with a high

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speed asynchronous communication interface 105 ("H.S. ASYNC INTRFCE") to support facsimile or external display screen operations. In addition, the application processor 48 may communicate data to an RS-232/RS-485 serial interface module 34 ("SERIAL INTERFACE"). However, it should be realized that certain communications operations, such as outgoing communications to a printer (not shown) for example, may occur under the control of the control processor 49. Even when the application processor 48 selects data for communication to a line printer, a typical printer speed, except in a graphics mode, would be sufficiently slow to allow the application processor 48 to operate in an intermittent, power saving mode. FIG. 6 consequently shows a second RS-232/RS-485 interface 106 ("SERIAL INTRFCE") coupled to a second data bus 107, which is further communicatively coupled to the control processor 49 to support the above described data communication operation via the control processor 49.

The data bus 107 is further shown as being coupled via a bus extension 108 directly to the application processor 48. The data bus extension 108 is particularly provided for direct data communication between the application processor and a data scanner 109 ("SCAN"), which may, for example, be a bar code reader. Because of the high rate at which data are generated by the operation of a data scanner, the data are most reliably received, processed and stored by the application processor 48. A scanning operation may consequently involve the operation of both the application processor 48 and the control processor 49. According

to one embodiment of the control circuit 80, the control processor 49 monitors the circuit function of the data scanner 109 to detect a control signal that indicates the event of a scanner trigger depression. The scanning operation results in a string of data appearing at the data bus 107 and the associated data bus 108. Since the application processor 48 is likely to be idle at the time of the occurrence of a trigger signal, the control processor places a "wake-up" signal on the control signal line 98 to activate the application processor 48. The control processor 49 further writes an 8-bit control character into the first latch 86. Upon completion of loading the control character into the data latch 86, the control processor 49 places a "one" signal on the character available line 91 to allow the application processor to read the control character from the latch 86. The application processor reads and decodes the control character in accordance with protocol instructions read from the ROM memory 56, for example. In the example of a scanner trigger indication, the decoded control character signals the forthcoming string of information to be received by the application processor 48 directly from the scanner 109 over the data bus 108. Hence, in contrast to being conditioned for the event of receiving data from the keyboard 49 or from the radio 81 (which data might preferably be received over the data latch 86), the application processor would in the event of scanned incoming data be conditioned to read the "event data" as a string of data directly from the data bus 108. The term "event data" is used to describe data relating to an event. Any time event data

requires processing, such event data would be routed to the application processor 48 either directly, as described with respect to the scanner data, or between the two processors 48 and 49, such as by the circuit 67 or a similar interface circuit. It should be understood that conditioning the application processor to receive a string of data directly via the bus 108 need not be limited to the receipt of the scanner data. Such conditioning is contemplated for any use of the terminal 10 which requires a high volume of data to be received and processed within a short period of time. Upon completion of the scanning operation, a trigger release signal is loaded into the first latch and communicated from the control processor 49 to the application processor 48. Upon receipt of the signal and completion of any data processing operations remaining as a result of the receipt of data via the data bus 108, the application processor instructs the control processor to apply a "wake-up" signal to the control signal line 98 upon occurrence of any specified event requiring processing of data. Thus, in one embodiment, the control processor 49 continues to control the application processor 48 by transmitting control codes to selectively enable or disable the application processor 48 to directly receive data via the data bus 108. The receipt of data by the application processor 48 is referred to as "direct" data input, since the contemplated transfer of data via the data latches 86 and 92 is bypassed.

FIG. 2 shows schematically one embodiment of electrical components of an exemplary terminal unit 10, and the interactive

relationship of such components to the application processor 48 or the control processor 49. FIG. 2 shows schematically a plurality of electrical components which are generally directly related to the functional elements discussed with respect to FIG. 6. In the embodiment shown in FIG. 2, the application processor 48 directly controls the previously referred to high speed asynchronous communications interface 105 and the RS-232/485 standards serial interface 34. The flash EPROM programmable read-only memory 58 is preferred to have no less than 256K byte storage capacity. The flash EPROM may supplement or even replace standard ROM, such as memory 56, which is preferred to have at least a 512K byte storage capacity. The ROM, if used, provides typical and normally non-variable data processing protocol instructions. Such ROM may include control instructions for standard display updating routines as well as for other routines which are typically implemented by standard keyboard instructions and which pertain to typical data input and output commands.

The random access memory 56 may be a semi-permanent static RAM type circuit. The memory may have a capacity of 512K bytes. The preferred data storage capacity provides sufficient storage for an on-board data base related to typical inventory or delivery route type information. In view of the portability of the terminal unit 10, an unexpected loss of battery power may bring about a significant loss of information unless the stored data are protected from destruction until full battery power is restored. For example, the terminal unit 10 may be returned at an initial

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signal of "low battery" to a battery charger unit (not shown) for a recharging operation and any stored data may be transferred, even while the battery 23 is being recharged, from the terminal unit 10 to a host computer (not shown).

Display 20 may be a graphic display having an array of 48 x 100 pixels. Typical menu or special graphic screen data may be pre-established for a particular terminal unit 10 or for an application group of such units and may be stored initially in the specific ROM 56 provided for the particular unit or units 10. As previously discussed, the updating of displayed data on the screen device 20 requires a significant amount of data processing. Typically, such data processing operations involve accessing permanently stored screen display information, such as from the ROM 56 or from the flash EPROM 58, the manipulation of such information, and temporary storage of such manipulated information in the random access memory 57. As shown in FIG. 2, the application processor 48 has direct functional control over the respective devices responsible for such data updating manipulations.

Contrast control is another function which is desirable in LCD display screen 20. In regards to FIG. 2, such a control may be integrally coupled to the VGA adapter circuit 54. The contrast of the LCD display screen 20 is typically set and adjusted by an operator and is a matter of choice. The contrast may be adjusted, for example, by a typical key depression or by a keyboard sequence given by an operator. Such control input executions are within the

scope of operations of the control processor 49. Thus, in response to an appropriate command from the keyboard 102, the display contrast may be changed without activating the application processor 48. The contrast display may be controlled as indicated in FIG. 2 by the functional coupling of the keyboard circuit 102 to the control processor 49, and the further coupling of the processor 48 to the contrast control circuit and then directly to the LCD display screen circuit 20.

In one embodiment, the LCD display screen 20 is equipped with a backlighting drive 62. Many warehouse operations, route delivery operations and even merchandising inventory operations are often performed under sufficiently poor lighting conditions, thereby requiring a backlighting source to be supplied as a standard feature of the LCD display screen 20. A backlight drive circuit 62 may be coupled through the MBUS 50 to the control processor 49. A backlight drive circuit for use in conjunction with the exemplary terminal unit 10 is described in copending patent application by S. E. Koenck et al., Serial No. 07/776,059, filed on October 11, 1991, which application is assigned to the assignee of the present application. Both the application processor 48 and the control processor 49 may interact with the backlight drive circuit 62 to provide for an operator controlled brightness control sequence to be communicated to the backlight drive 62.

It should be realized that the control circuit 67 as an ASIC may also include, besides the timing function circuits for the real time clock and its functions, the clocking signals to each of the

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two processors 48 and 49. The control circuit 67 may also provide the already described data communication functions between the application processor 48 and the control processor 49, as represented in FIG. 6 by the two latching circuits 86 and 92. The function by the control processor 49 to activate or "wake up" the application processor for data processing operations is accentuated in the representation of the "wake-up" feature by the separate function line 98 in FIG. 2. In one contemplated embodiment, the control circuit 67 may include integrally a switching circuit function for separately switching the application processor 48 off or on, as indicated in FIG. 9 by the function blocks "#1 OFF WAIT" and "#1 ON". A switch in the integrated control circuit 67 may perform the switching operation by selectively interrupting and reestablishing the clocking signal to the application processor 48. In another embodiment, the application processor 48 may provide a shutdown status signal to the control processor 49 and shut itself down. The control processor 49 subsequently returns the application processor 48 to an active state upon occurrence of any event which requires the operation of the application processor 48. The process flow diagram of FIG. 9 generally depicts operational procedures between the application processor 48 and the control processor 49.

Further in reference to FIG. 2, a trigger control signal of the scanner module 41 may be received by the control processor 49. However the data flow from the scanner module 41 would be received directly by the application processor 48 for further processing and

storage. Input signals which are received at speeds within the operational capability of the control processor 49 are received by and transferred through the control processor 49. For example, key depression signals from the keyboard 49 are generally received directly by the control processor 49. The keyboard for the terminal unit 10 referenced herein, as indicated in FIG. 2, may be

a 6x8 key matrix. Because the real time selection of a key by an operator is slow in comparison to the processing speed of even the slower control processor, the interpretation of which key has been selected may be made by the control processor 49. An "event" indication character communicated to the application processor 48 may already reflect which of the available functions of a particular key has been selected. The preprocessing of slow occurring events limits the operational periods of the application processor 48.

The control processor further controls an input to an audible alarm circuit 63 ("BUZZER"). An audible alarm, a slow occurring event, generates a signal to alert an operator of an alarm condition or to indicate that a processing operation has been completed. For example, when the application processor 48 has received a string of data from the scanner module 41, and has further processed the received information to verify its correctness, the application processor 48 may communicate an acceptance code to the control processor 49 and be shut down from further operation. The control processor will then routinely

operations, which include periodic monitoring functions. The control processor 49 controls the activation or reactivation of the application processor 48. However, the application processor 48 processes the parameters and feeds to the control processor 49 the respective instructions that control the control processor 49. The application processor 48 is therefore, according to one embodiment, the one device which accesses the operations protocol of the terminal unit 10 from either the ROM or the flash EPROM devices 56 or 58.

Referring now to FIG. 9, the depression of the power switch by an operator, physically starts the terminal unit with a cold start at a block 301. The turn-on starts the clocking signal and the reset of both the control and application processors 48 and 49. The control processor 49 may reset the application processor 48 at a block 303. The reset operation starts the apparatus at a block 305 with an initialization sequence of communications between the application processor 48 and the control processor 49. During the initialization, the application processor 48 retrieves from its program storage default values, such as for a battery threshold value, and transfers the respective default value to the control processor 49 at a block 307. The control processor retains the default value and uses it in its further operations to operate the power control circuit 64. Other initialization functions may be performed, such as, for example, setting an initial contrast value on the LCD screen display 20 at a block 309, and determining whether or not the backlighting function is to be activated at a

block 311. The application processor 48 further may retrieve data from memory 56, 57 or 58, and manipulate such data in a manner to indicate on the screen that the unit 10 is operational. Once the terminal unit 10 is initialized, the application processor 48 communicates to the control processor 49 that it is assuming its rest state at a block 313, and is shut off pending the occurrence of an event.

Upon occurrence of an event at a block 315, such as a "battery low indication" or the depression of a key by an operator, the control processor 49 causes the application processor 48 to turn at a block 317. Typically the clock signal to the application processor 48 may be provided by a control signal applied to the control device 67, or the application processor may be otherwise enabled, such as by an enable signal applied to the control signal line 98. Upon being activated, the application processor 48 communicates with the control processor 49, such as via the interface circuit 24 as described above with respect to FIG. 6, to request at a block 319 data relevant to the type of event that has occurred. After receiving the respective communication from the control processor 49, the application processor 48 tests the received information as to the type of event and proceeds to process data as required according to the program. FIG. 9 shows three typical events of a large number of possible programmed events for which the application processor 48 may be activated. A typical key depression detected at a block 321 may result in reading the value of the depressed key, at a block 323, from the

second data latch 92 as described with respect to FIG. 6, or from an equivalent register of the control device 67 in FIG. 2. The information then results in the retrieval of data regarding the addresses of pixels which will be changed to a logical "high" to depict the information on the LCD display screen 20, at a block 325 the respective data being transferred to the respective circuit elements of the display screen 20. Thereafter, the application processor communicates to the control processor 49 that the instructions have been executed and is shut down to await a further activation by an event at block 315 and an instruction at block 317. The shutdown of the application processor 48 may be initiated either by the application processor 48 itself or by the control processor 49. Because the start-up or activation of the application processor 48 is initiated by the control processor 49, it may be desirable to disable the application processor 48 through the control processor 49.

Another typical event for activating the application processor 48 may be the detection of a low battery indication at a block 327 in response to a threshold value transferred by the application processor 48 to the control processor 49 during the described start-up procedure. The protocol may require that the application processor 48 verify the low battery indication by providing its own comparison check at a block 329. Because of an impending shutdown due to a low battery indication, the application processor may complete any operation if the low battery indication is still within tolerable limits or may suspend further data processing

because of risk of errors. The application processor may further display a low battery indication on the LCD display screen 20 at a block 331 and then be shut off pending further event instruction as described above.

Another type event may be a special function key instruction such as the indication that a menu operation has been selected at a block 333. The application processor 48 proceeds to access a designated program routine corresponding to the requested menu choice ("RETRIEVE MENU DATA"). The respective program instructions are executed at a block 337, and the result or completion of the routine is displayed on the LCD display screen 20 at a block 339. The displayed result may be preceded by a repetitive interactive data transfer between the application processor 48 and the control processor 49, for example, when the menu choice requires the transmission of displayed information to a host computer. In such an event the application processor 48 may transfer the displayed information character by character to the control processor 49. The control processor 49 in turn activates the radio interface and transfers the information string to the radio interface to be transmitted in accordance with the program instructions interpreted by the application processor 48. FIG. 9 shows an error trap at a block 341 to which the program instructions proceed if an event code is not recognized by the programmed event descriptions and resulting processing routines of the application processor 48 for the particular application of the terminal unit 10. The data processing operations performed by the application processor 48

generally require less than 10 milliseconds. Thus, on the average, operations including the processing of keystrokes and the associated display manipulations require less than one fiftieth of the average operational period of the terminal unit 10. Substantial power savings are consequently achieved by selectively de-activating and re-activating the application processor 48 for preprogrammed events which require the execution of the respective data manipulations at a speed not obtainable by the control processor 49.

Further in reference to FIG. 9, if none of the event tests recognize the particular code supplied to the application processor 48, an event error trap routine at block 341 is used to inform the operator of the error condition. Such a routine may, for example, instruct the operator to again enter the most recently requested operation, and may include an audible warning from the buzzer. Various changes in the described control sequence may be implemented. Certain routines may be implemented at the described slower speed by the control processor 49 directly, while the application processor 48 remains deactivated. Further, other microprocessor devices may be chosen for the application and control processors, respectively. The described microprocessor devices are particularly suitable for various operations that are performed by the terminal unit 10 in the above-referred to operations.

FIG. 10 illustrates a portion of the software protocol stack 401 that runs on one of Norand Corporation's Portable Data

Collection Terminal Units, Model No. TM 1100 (See attached APPENDICES B and C). Specifically, the MAC (Medium Access Control) layer 403 is responsible for providing reliable data transmission between the terminal unit and any other node or device in a mobile computer network. When a radio module (e.g., Norand RM40 RF Module) is attached to the terminal unit and powered up, the MAC layer 403 and a Glue Logic Layer 405 are transferred to flash memory in the radio module. The Glue Logic Layer 405 controls the microprocessor in the radio module so that it is able to communicate with the high speed main microprocessor of the terminal unit. Generally, the Bridge Layer 407 organizes the nodes or terminals of the mobile computer network into an optimal spanning, routes data between any two nodes or terminals in the network, and provides data package storage to facilitate sleeping terminals. Appendix D provides an exemplary computer program listing of the software protocol stack 401 of FIG. 10 (Bridge Layer at pp. 1-33; MAC Layer at pp. 34-51; Glue Logic Layer at pp. 52-59). These protocol layers are actually subgroupings of the protocol stacks illustrated in FIGS 1B and 1C.

FIG. 11 shows an exemplary local area network (LAN) illustrating the roaming characteristics of the portable data collection terminals. Specifically, the illustrated LAN consists of a host computer 510, multiple access points 512, 514, 516 and a mobile computing device (MCD) 518. The MCD 518, a portable data collection terminal, is communicatively coupled to the host computer 510 through an access point 512. Although only one MCD,

MCD 518, is shown typically a plurality of MCDs would exist on the LAN. The MCD 518 communicates with the host computer 510 through the access point 512 to which it is connected.

There are two situations in which the MCD 518 becomes disconnected from the network 501. First, where the MCD roams out of the range of one access point, such as access point 512, into the range of another point, such as access point 514 as is shown by the dashed MCD 518 position. Alternatively, MCD 518 may enter a sleep mode where the radio transceiver is powered down. The sleep mode provides for power savings and is a desirable mode of operation is needed.

The MCD 518 and the access point 512 communicate in a structured manner, where the MCD 518 transmits a request-for-poll (RFP), the access point 12 responds with a poll, the MCD 518 then transmits its data, and the access point 512 responds with an acknowledge (ACK) signal if the data message is finished or with another poll if there is still more data to be transmitted. One data message from the MCD 18 to the access point 512 may consist of several POLL-DATA sequences, where each DATA transmission is a fragment of the entire data message. To initiate such communication exchange, channel access protocols must be established.

FIG. 12 shows the process implemented by a mobile computing device when it has a message to transmit to the host computer. A MCD wakes up at a block 551 when it has a data message to transmit to the host computer. This wake-up can occur at any possible

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moment in time, i.e., a random time. After waking up, the MCD senses, at a block 553, the communications channel for a predetermined time, which is greater than or equal to the maximum interpoll gap time. In this context, a maximum interpoll gap time is defined as the maximum time between poll messages transmitted from the access point to the MCD. This assures the MCD that a transmission from the access point to another MCD will occur within the sensing time if the channel is currently being used. If, at a block 555, the channel is clear for the interpoll gap time, the MCD transmits a RFP at a block 559, and the communications sequence begins. If, at block 555, the channel is busy during the interpoll gap time, the MCD waits a fixed time period at a block 557 and senses the channel at block 553 as before.

Because the MCD wakes up at some random time to send data to the host, the probability of collision with the transmission of another MCD is extremely small. By sensing the channel for a fixed period of time and waiting for a fixed period of time to retry transmission, the random nature of transmission attempts is retained even after a busy channel is sensed. For a collision to occur in this scenario, two MCDs would have to wake up at the exact same moment in time, the probability of which is extremely small.

FIG. 13 shows a process similar to that of FIG. 12, except that a retry counter implementation is used. Upon waking up to transmit at a block 601, a MCD resets a retry counter to zero at a block 603, indicating that it is the first attempt to communicate on the channel. If, at block 607, the channel is determined to be

channel sensing or between a busy channel sense and a further channel sense should be greater than or equal to the time between SYNC messages minus the maximum interpoll gap time. This assures that a SYNC message will be received each time before the MCD attempts to sense the channel and transmit. In addition, after receiving a sync signal, the MCD listens for an interpoll gap time 659 to determine if the channel is clear, at blocks 659 and 661. If clear, the MCD transmits an RFP at a block 663.

FIG. 15 shows a process similar to that of FIG. 14, except that a retry counter implementation is used to control the number of retry attempts. Upon waking up to transmit at a block 701, a MCD resets a retry counter to zero at a block 703, indicating that it is the first attempt to communicate on the channel. Each time the channel is sensed and is determined to be busy, the retry counter is incremented at a block 717. Once the retry counter reaches a predetermined MAX value at a block 719, the MCD stops trying to transmit and goes back to sleep at a block 723, for some relatively long period of time before trying to transmit again. This procedure allows a terminal to save power if the channel is heavily loaded by sleeping until the channel may be less heavily loaded. In addition, if the channel is busy but the retry counter has not reached the MAX value, the MCD may either sleep or wait for a fixed period of time at a block 721. Although a fixed period of time is desirable, a random or pseudo-random back-off might also be used.

FIG. 16 is a flow diagram illustrating a channel access

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protocol using a pseudo-random number generator according to another embodiment of the present invention. Upon waking up to transmit at a block 751, a MCD generates a pseudo-random number (e.g., 5-8 microseconds) at a block 753. The MCD then senses the communication channel for a few microseconds at a block 755. If the channel is determined to be clear at a block 757, the MCD determines whether the pseudo-random time period has expired at a block 757. If it has expired, the MCD transmits an RFP at a block 761, and the communications sequence begins. If the pseudo-random time period has not expired, the MCD again senses the communication channel for a few microseconds determined at a block 755 to determine if the channel is clear at block 757, i.e., repeating the above.

If the channel is determined to be busy at block 757, the MCD increments a retry counter at a block 763. If the retry counter has not reached a predetermined maximum value at a block 765, the MCD waits for a pseudo-random time (e.g., 10 milliseconds) at a block 769 and then generates another pseudo-random number at block 753 and repeats the above procedure. Once the retry counter reaches the predetermined maximum value, at block 765, the MCD quits trying to transmit and goes to sleep for a longer period of time at a block 767, before reawakening at block 751 to retry the transmission.

FIG. 17 shows the basic communication structure in one embodiment of the present invention. Access points periodically transmit a series of SYNC messages such as 809-813, while allowing

time for communication exchanges during the periods 815-819 between SYNC messages. In general, the SYNC message itself takes much less time than the amount of time allocated for communication between SYNC messages. The time allocated for a SYNC message and for subsequent terminal communication (i.e., until another SYNC message is transmitted) is depicted by periods 803-807.

FIG. 18 shows a series of exemplary communication exchanges and channel access attempts where three MCDs are attempting to communicate in the same general time frame. The three units attempting to communicate are referred to as unit 1, unit 2, and unit 3. Unit 1 wakes up first at 831, in the first time interval 815. It must wait until it receives a SYNC message at 811, so it cannot attempt to transmit in time interval 815. Unit 2 is the next to wake up at 833, also in time interval 815. As with unit 1, unit 2 cannot transmit until a SYNC 811 is received, and therefore cannot transmit in time interval 815.

After the timer set by unit 1 when it initially woke up expires, SYNC message 811 has been received by unit 1. Thus, unit 1 can listen to the communications channel at 841 for the maximum interpoll gap time, determine a clear channel, and begin its communications sequence at 843, all in this time interval 817. The timer initially set by unit 2 also expires during time interval 817, and unit 2 has therefore received the SYNC message 811 and senses the communications channel at 847. However, unit 1 has not yet finished its transmission when unit 2 senses the channel for the maximum interpoll gap time. Thus, unit 2 must defer

transmission, and waits until time interval 819 to retry communication.

Meanwhile, also in time interval 817, unit 3 initially wakes up to transmit at 845. Unit 3 must wait for a SYNC before attempting to transmit, so it does not transmit in the time interval 817.

In time interval 819, after the SYNC message 813, unit 2 and unit 3 have both received a SYNC message and can sense the channel to attempt transmission. In this case, unit 3 listens to the channel at 861 slightly before unit 2 senses the channel at 863, such that the channel is not busy when unit 2 begins to sense the channel. However, after unit 3 has sensed the channel for the maximum interpoll gap time, it begins communication on the channel at 865. Unit 2 finishes listening to the channel, also for the maximum interpoll gap time, after unit 3 has begun its communication, so unit 2 must defer communication. Unit 3 ends its transmission at 867. Finally, after SYNC message 869 in time interval 871, unit 2 senses an idle channel at 873 and transmits its communication to the access point at 875. Unit 2 ends its transmission at 877. This sequence illustrates the interpoll gap time channel sense and the wait to transmit until after a SYNC message has been received.

The operation of the protocol of the present invention takes advantage of the inherently random wake-up time of a mobile computing device in a local area communications network. Rather, than performing a random back-off routine, the time of wake-up is

used to ensure random communications attempts, thereby preventing collisions due to many terminals attempting to transmit immediately after a certain common event. This is done by preserving the random wake-up time, adding a fixed amount of time to the time of wake-up in back-off procedures. The protocol of the present invention eliminates the need for random number generation and the implementation of random back-off algorithms.

FIG. 19 is a timing graph illustrating an exemplary communication exchange between a portable data terminal 901 and an access point 903. Upon determining that the channel is clear, the portable data terminal 901 begins by transmitting an RFP (request for poll) frame 905. After an interframe gap time 923, the access point 903 responds with a POLL frame 907 to indicate to the portable data terminal 901 that it is available to receive data. The portable data terminal 901 then sends a DATA frame 909. The access point 903 acknowledges receipt of DATA frame 909 with a POLL frame 911. The portable data terminal 901 then transmits DATA frame 913 which indicates that data transmission is complete. The access point 915 then transmits a CLEAR frame 915 to acknowledge receipt.

A channel reservation scheme is used to generally restrict channel access contention to RFP frames. Each frame transmitted during the communication exchange contains a channel reservation field (e.g., field 931 in POLL 907) which may indicate either the number of outstanding frames or the amount of time required to transmit the outstanding frames.

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This scheme enables other terminals attempting to access the busy channel to determine the actual amount of time during which they may sleep. Sleeping, i.e., or powering-down the radio for the duration of the channel reservation period (i.e., until the channel becomes clear) conserves battery power and aids in collision avoidance. Further, channel reservation may be implemented with the other channel access embodiments discussed above during heavy communication traffic. In other words, channel reservation may supplement other channel access protocols when terminals using those protocols are continuously failing to gain access to the channel.

FIG. 20 is a flow diagram illustrating an embodiment of the channel access reservation scheme described above. A portable data terminal (or mobile computer device ("MCD")) wakes up to transmit data at a block 951. It then senses the channel for an interpoll gap time at a block 953 before determining if the channel is clear at a block 955. If the channel is clear, the portable data terminal transmits an RFP and the communication sequence begins (e.g., that shown in FIG. 19). If the channel is busy, the portable data terminal listens for the channel reservation information on the channel at a block 959, and calculates the time that it should "sleep" and powers down at a block 961. At the end of the calculated sleep period, the portable data terminal wakes up to transmit at a block 963 and repeats the process by sensing the channel for an interpoll gap time at block 953.

FIG. 21 shows a radio card 1110 and a receiving device 1111 built in accordance with the present invention. The radio card 10 has a housing 1113 inside which is a completely operation radio transceiver not shown. The receiving device 1111 in this embodiment of the present invention uses a pair of opposed slots 1114 to receive and guide the incoming radio card 1110.

The radio card 1110 has a pair of antenna contacts 1115 positioned along the edge of the housing 1113. The receiving device 11 has a corresponding pair of antenna contacts 1116. As can be seen in FIG. 22, when the radio card 10 is inserted into the receiving device 1111 the antenna contacts 1115 on the radio card housing 1113 electrically encounter the corresponding set of antenna contacts 1116 positioned on the receiving device 1111. The antenna contacts 1116 on the receiving device 1111 are connected to an antenna cable 1118. The antenna cable 1118 is in turn connected to an antenna not shown. Thus, when the radio card 1110 is completely inserted into the receiving device 1111 the radio card 1110 automatically is connected to an antenna.

Referring again to FIG. 21, a radio card 1110 may have antenna contacts 20, shown in dashed lines, located at different positions on the housing 1113. Similarly, the receiving device 1111 may have several additional pairs of antenna contacts 22. The additional pairs of antenna contacts 22 on the receiving device 1113 can be used to allow access to several different antennas depending on the type and frequency of radio communication to be utilized by the radio card 1110. This access is accomplished through additional

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antenna cables 1123 attached to the additional contacts 1122. Thus, if the receiving device 1113 is part of a hand held computer terminal which has more than one antenna attached or built in, different pairs of contacts 1116 & 1122 can be used to allow access by the radio card to the different antennas depending upon the frequency and range characteristics of each antenna. While a radio card 1110 may only operate at one frequency and thereby only need one antenna and therefore only have one pair of antenna contacts, the receiving device 1111 still may have several pairs of antenna contacts 1116 & 1122 all but one of which do not correspond to any pair of radio card 1110 antenna contacts 1115.

Referring to Figs. 23 and 24, when the radio card 10 is inserted into the receiving device 1111 an interface between the radio card 1110 and the receiving device 1111 is produced. The receiving device 1111 has a plurality of pins 1130 which form the male portion of a connector. The radio card 1110 has a corresponding plurality of holes 1131 which form the female portion of the connector and which engage the pins 1130. The pins 1130 are connected to the computer terminal not shown by a series of electrical connections 1133 such as wires or electrical ribbon. The holes 1131 in the radio card 1110 are electrically connected to the radio. When the pins 1130 are engaged in the holes 1131, electrical signals can be exchanged between the radio card 1110 and the computer terminal. The electrical signals can be in the form of information exchange, power supply or both.

The radio card 1110 of Figs. 21-24 might also be a modem card

not shown. In this embodiment, the connections would be the same as previously described with the only difference being that instead of the contacts connecting the modem card to a radio antenna, the modem card would be connected to a traditional telephone line, a cellular phone or an antenna for a cellular phone if the cellular phone was built within the modem card.

Referring to Figs. 25 and 26, a computer terminal 1140 is shown built in accordance with the present invention. The computer terminal 1140 has a slot 1142 for receiving a radio card 1144. The user of the computer terminal 1140 lifts up a flexible cover 1146 and inserts the radio card 1144 into the slot 1142. The radio card 1144 engages with the computer terminal 1140 in a similar manner as described in Figs. 21-24. The radio card 1144 has a pair of antenna contacts 1148 which will engage with a corresponding pair of contacts inside the computer terminal 1140. The pair of antenna contacts inside the computer terminal are connected to a radio antenna not shown.

Referring to FIG. 27, another embodiment of the present invention is shown. The radio card 1150 has two pairs of antenna contacts 1152 & 1153 which will encounter respectively two pair of antenna contacts 1155 & not shown on the receiving device 1158. This embodiment accommodates a radio card 50 which can operate at two different frequencies which require two different antennas. Standardization of antenna contact position with antenna type is anticipated and covered by the present invention.

Referring to Figs. 28-32, another embodiment of a computer

terminal 1160 built in accordance with the present invention is shown. The computer terminal 1160 has a removable end cap 1162. When the end cap 1162 is removed, a slot 1160 is revealed which is used to receive a radio card 1166. The slot 1164 in the computer terminal 1160 has three pairs of antenna contacts 1167, 1168 and 1169 which are respectively connected to three different radio antennas 1171, 1172 and 1173. The radio card 1166 in this embodiment only has one pair of antenna contacts 1175. Thus, when the radio card 1166 is inserted into the slot 1164, the antenna contacts 1175 will match up to the antenna contacts 1167 and the radio will utilize the internal antenna 1171. The external antenna 1173 and the other internal antenna 1172 will not be used by this particular radio card 1166.

Referring now to FIG. 33, still another embodiment of a computer terminal 1180 built in accordance with the present invention is shown. A communication card 1185 is inserted into the computer terminal 1180. The card 1185 can either be a radio card or a modem card. The card 1185 has a set or pair of contacts 1187 which encounter a set or pair of contacts 1188 disposed on the receiving portion of the computer terminal 1180. The contacts 1188 are electrically connected to a switching matrix 1190, thus the radio card or modem card 1185 is electrically connected to the switching matrix 1190.

The switching matrix 1190 is connected to a plurality of antennas 1192, 1193 and 1194 and to a telephone jack 1195. The switching matrix 1190 is used to electrically and selectively

connect the radio or modem card 1185 to the appropriate antenna or to a telephone line. The switching matrix 1190 is controlled by the control microprocessor 1198 of the computer terminal 1180. The control microprocessor interrogates the card 1185 to determine what kind of card it is and to determine what antenna or telephone connection it needs. The control microprocessor then signals the switching matrix 1190 which connects the card 1185 to the appropriate antenna 1192, 1193 or 1194 or to the phone jack 1195.

Figs. 34, 35 and 36 illustrate another embodiment wherein a computer device 1211 utilizes a radio card 1210 built in accordance with the present invention. The computer device 1211 has a housing 1212. Inside the radio card 1210 is a completely operation radio transceiver not shown. The computer device 1211 has an opening 1214 in the housing 1212 through which the radio card 1210 can be inserted into the computer device 1212. In the present embodiment of the invention, the receiving means for the computer device is a slot 1215.

When the radio card 1210 is inserted into the slot 1215 in the computer device 1211 an interface between the radio card 1210 and the computer device 1211 is produced. The computer device 1211 has a plurality of pins not shown which form the male portion of a connector. The radio card 1210 has a corresponding plurality of holes not shown which form the female portion of the connector and which engage the pins. The pins are connected internally and electrically to the computer device 1211 by a series of electrical connections such as wires or electrical ribbon. The holes in the

radio card 1210 are electrically connected to the radio transceiver. When the pins engage the holes, electrical signals can be exchanged between the radio transceiver inside the radio card 10 and the computer device 1211. The electrical signals can be in the form of information exchange, power supply or both. The radio card 1210 includes antenna contacts 1217 to engage corresponding radio antenna contacts that are connected to an appropriate antenna.

The computer device 1211 includes a cap 1220 which is designed to matingly engage the opening 1215 in the housing 1212 of the computer device 1211 and thereby cover the slot 1215 used to receive the radio card 1210. A flexible band 1222 attaches the cap 1222 to the housing 1212 of the computer device 1211. One end of the band 1222 is connected to the cap 1222 while the other end is attached to the housing 1212. A handle 1224 helps assist the removal of the cap 1220 from the housing 1212 of the computer device 1211.

The cap 1220 is constructed of a closed cell foam material with high air content for low dielectric losses. Alternatively, a quality dielectric material may be used to reduce the size of the antenna structure. The cap 1220 when made of a foam material helps to protect the radio card from the physical trauma typically associated with computer devices of these types. Additionally, as will be discussed in further detail below, the cap 1220 helps to environmentally seal the opening 1214 preventing harmful material from the outside such as dust or moisture from reaching the radio

card 1210 and helps to reduce the escape of electronic noise from the housing 1212 created by the radio card 1210 and computer device 1211. As will be discussed below, a grounded metal shield covering a portion of the cap 1220 is used to reduce the escape of electronic noise.

While the cap 1220 helps to seal the opening, protect the radio card 1210 and hold the radio card in place, the primary function of the cap is to provide the radio card 1210 access to an appropriate antenna or antennas. The connection of the radio card 1210 to the antenna is made through the cap 1220. The antenna or antennas can be embedded in the cap 1220, embedded in the band 1222 or even attached to, mounted on, or embedded in the housing 1212 of the computer device 1211.

Referring now to Figs. 37 and 38, a computer device 1230 built in accordance with the present invention is shown with a cap 1234 engaged in the opening of the housing 1232 wherein a radio card can be inserted. A band 1236 is attached to both the cap 1234 and the housing 1232. The band 1236 helps prevent the loss of the cap 1234 when the cap 1234 is not engaged in the housing 1232 of the computer device 1230.

Referring now to Figs. 39 and 40, the cap 1232 is shown engaged with the housing 1232 of the computer device 1230. The cap 1234 includes an outwardly extending lip 1236 which helps to environmentally seal the opening in the housing 1232 preventing harmful material from the outside such as dust or moisture from reaching the radio card 1240 which has been inserted into the

computer device 1230. When the cap 1234 is completely inserted or fully engaged in the housing 1232, the lip 1235 sealingly engages the housing 1232.

Embedded in the cap 1234 is an antenna 1250. The antenna 1250 is connected to the radio card 1240 through contacts 1251 and 1252 disposed on the cap 1234 and contacts 1241 and 1242 disposed on the radio card 1240. Contact 1252 is the ground contact for the antenna 1250 and is connected to the end of the antenna 1250. Contact 1242 is the ground contact for the radio card 1240. Contact 1251 is the signal contact and is connected to the antenna 1250 a short distance from the end of the antenna 1250. Contact 1241 is the signal contact for the radio card 1240.

Contact 1251 and contact 1241 are disposed on the cap 1234 and the radio card 1240, respectively, such that the contacts engage each other when the cap 1234 is inserted into or engaged with the housing 1232 of the computer device 1230. Similarly, contact 1252 and contact 1242 are disposed on the cap 1234 and the radio card 1240, respectively, such that the contacts engage each other when the cap 1234 is inserted into or engaged with the housing 1232 of the computer device 1230. The contacts shown in the present embodiment are of the metal button type wherein the connection is made when the two metal surfaces meet. Many variations of the contacts are possible including the use of male/female connections and spring type contacts.

A shield 1248 is disposed around the bottom portion of the cap 1234 and is used to reduce the escape of electronic noise.

Typically in computer devices of this type, the inside of the housing of the computer device is shielded. Additionally, the area immediately surrounding the radio device such as a radio card may also be shielded. By shielding the cap 1234, the integrity of the housing and radio shields are not breached by the opening used to insert and remove the radio card. The shield 1248 is connected to the antenna ground contact 1252 on the cap 1234. A hole 1259 in the shield 1248 allows the signal contacts 1251 and 1241 to engage without being grounded.

Referring now to FIG. 41, the cap 1234 is shown embedded within which are two antennas 1260 and 1262 designed to receive and transmit different radio frequency signals. The first antenna 60 and the second antenna 1262 are both connected to a common ground contact 1267 which is connected to the shield and which engages the ground contact 1277 on the radio card 1270. The first antenna 1260 is connected to a first signal contact 1265 and is disposed on the cap 1234 to engage a first signal contact 1275 disposed on the radio card 1270. Similarly, the second antenna 1262 is connected to a second signal contact 1266 and is disposed on the cap 1234 to engage a second signal contact 1276 disposed on the radio card 1270. Thus the radio card 1270 will use a signal via contact 1275 or via contact 1276 depending upon which antenna it would like to use. Which antenna it would like to use is dependent upon the desired frequency upon which it want to transmit and receive.

The radio card 1270 as shown has three contacts 1275, 1276 and 1277. However, if the radio transceiver in the radio card 1270 is

designed such that it would only be able to transmit and receive signals which correspond to the first antenna 1260, then it would not need to have contact 1276 and it could be left off. Similarly, if the radio card 1270 were only going to use second antenna 1262 then contact 1275 could be omitted. Thus, standardizing contact position with respect to antenna type allows for flexibility in cap usage with various radio cards such that only appropriate antennas will be connected to the radio card.

Referring to FIG. 42, two antennas 1280 and 1282 are embedded in the cap 1234. In this embodiment built in accordance with the present invention, the two antennas 1280 and 1282 not only share a common ground contact 86 which engages the ground contact 1296 of the radio card 1290, but they also share a common signal contact 1285 which engages the signal contact 1295 on the radio card 1290. Thus, both antennas receive and transmit signals using the same two contacts: This embodiment requires a radio card 1290 which can filter the different signals and thus use the signal from the desired antenna while ignoring the signals which arrive via the other antenna.

Referring to FIG. 43, a computer device 1211 built in accordance with the present invention is shown which is designed to implement an antenna diversity scheme. A first antenna 1301 is embedded in the cap 1220. A second antenna 1302 is shown embedded in the band 1222. As discussed in the embodiment as shown in FIG. 8, the two antennas 1301 and 1302 share a common ground contact 1307. The first antenna 1301 is connected to a signal contact

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1311 is similar to the second antenna 1312 and both are designed to transmit and receive similar radio frequency signals and are perpendicular with respect to each other such that an antenna diversity scheme can be implemented. The antennas 1311 and 1312 are connected to the contacts 1305, 1306 and 1307 through the cap 1220 and through the band 1212.

Referring to FIG. 46, the embodiment of FIG. 44 is shown with the only differences being that the first antenna 1321 and the second antenna 1322 are positioned slightly differently and the antennas are designed to transmit and receive different radio frequency signals. Thus, the radio card uses the signal on contact 1305 when it wants to receive signals via the first antenna 1321 and uses the signal on contact 1306 when it wants to receive signal via the second antenna 1322.

In Figs. 43, 44 and 46, the portion of the connection between the contacts 1305, 1306 and 1307 and the antennas which pass through the band 1212 are shown schematically as wires. In the best mode of the present invention, the transmission of the signal through the band 1212 would be accomplished through the use of a micro shield strip 1330 as shown in FIG. 45. The micro shield strip consists of several conductive ribbons running the length of the band 1212 and separated by the non-conductive material of the band 1212. A wide top ribbon 1333 and a wide bottom ribbon 1334 are used to sandwich two smaller ribbons 1336 and 1337. The smaller ribbons 1336 and 1337 are used to transmit the antenna signals and are connected to contacts 105 and 106 respectively.

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processing unit functionality of each radio is too different, additional separate processing units may be included. Finally, the MCD (the portable data collection terminal) might also be designed to receive multiple communication modules.

In addition, the base module may interrogate the selected ("inserted") communication module(s) to determine which antennas to interconnect. Alternatively, the communication modules may interrogate the base module and request from the available antennas. Where a suitable antenna is not available, an external antenna connector is selected. Available antennas may be installed inside or on the outside of the base unit. Of course the antennas might also be selected via the physical communication module connectors as described below.

It should be realized that various other changes and modifications in the structure of the described embodiment would be possible without departing from the spirit and scope of the invention as set forth in the claims.

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(b) sensing the communication channel for a first predetermined time;

10 (c) if during the sensing of the communication channel the channel remained clear, transmitting to the access point; and

(d) if during the sensing of the communication channel the did not remain clear, waiting for a second predetermined time, and branching to step (b).

²
10. The method of claim ¹~~9~~, wherein said first predetermined time is greater than or equal to the maximum time between the access point's transmissions when engaged in a communications exchange.

³
11. In an RF communications network having a communication channel, an access point and a portable data collection terminal, wherein the portable data collection terminal having a transceiver which may be selectively powered up or down to conserve energy, a method used by the portable data collection terminal for gaining access to the communication network, comprising the steps:

(a) powering up the transceiver;

(b) resetting a retry count;

10 (c) sensing the communication channel for a first predetermined time;

(c) if during the sensing of the communication channel the channel remained clear, transmitting to the access point, else, if the channel did not remain clear, incrementing a retry count; and

15 (e) if the retry count is less than a threshold value,
branching to step (c), else, powering down the transmitter for a
period of time before branching back to step (a).

4
12. In a local area communications network having a
communication channel, a host computer, an access point, and a
portable data collection terminal, wherein the portable data
collection terminal has the capability to enter a sleep mode when
5 not transmitting or receiving, and the access point periodically
transmit SYNC messages, a method used by the portable data
collection terminal for gaining access to the communication
network, comprising the steps:

10 (a) waking up when data is available for transmission to the
host computer;

(b) waiting for a first predetermined time in order to
receive a SYNC message from the access point;

(c) sensing the communications channel for a second
predetermined time to determine if the channel is busy;

15 (d) transmitting a request for poll to the access point if
the channel is clear for the second predetermined time; and

(e) if the channel is busy during the second predetermined
time, repeating step (b).

5
13. The method of claim ⁴12, wherein said first predetermined
time is greater than or equal to the time between SYNC messages
minus the maximum interpoll gap time.

6
14. The method of claim ⁴12, wherein said second predetermined fixed time is greater than or equal to the maximum interpoll gap time.

1
15. A method used by a sending device for beginning a data exchange over an RF communication link with a polling device, wherein the polling device has an interpoll gap time, comprising the steps of:

5 (a) identifying that the RF communication link is clear throughout a period which is at least as long as the interpoll gap time; and

(b) transmitting a request for poll frame.

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16. The method of claim ⁷15 further characterized by the steps of:

(a) generating a pseudo-random number corresponding to a first pseudo-random time which is at least as long as the interpoll gap time;

15 (b) sensing the channel for a time substantially shorter than the first pseudo-random time;

(c) repeating step (b) until the channel is detected as being busy, or the channel is detected as being clear at every sense until the first pseudo-random time is reached;

20 (d) if the channel is detected as being busy, executing a second pseudo-random time delay back-off and returning to step (a); and

(e) if the channel has been detected as being clear for the entire first pseudo-random time period, transmitting a request for poll frame.

9
11. The method of claim 8 wherein step (d) further comprises the step of incrementing a retry counter and testing said retry counter such that a second pseudo-random back-off and retry will not be performed if said retry counter is above a predetermined threshold value.

18. In a communication network having a first and second subnetwork, a portable data collection terminal comprising:

a base processing unit capable of operating per a first set of communication software routines;

a first selected one of a plurality of radio transceivers, each having different operating characteristics;

a second selected one of a plurality of radio transceivers, each having different operating characteristics; and

a communication process capable of isolating the base processing unit from differences in the operating characteristics of the first and second radio transceiver.

19. The portable data collection terminal of Claim 18 wherein the communication processor comprising:

a first processing unit capable of isolating the base processing unit from the differences between the first selected one